Processor Performance, Packaging and Reliability Utilizing a Phase Change Metallic Alloy Thermal Interface System

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Introduction

With average processor core-level power densities approaching 300 W/cm^2 and nearly 50% of the overall processor junction-to-case thermal resistance budget consumed at the first level thermal interface (TIM1), the use of an all-metal interfacial thermal path is highly desirable. Phase Change Metallic Alloys (PCMAs), unlike eutectic solders, are well-suited as a TIM1 thermal interface between materials of dissimilar Coefficients of Thermal Expansion (CTEs), such as a copper lid and silicon die. PCMAs offer superior thermal performance due to their high thermal conductivities and low contact resistance, resulting from excellent surface wetting. Reworkability, ease of handling, and a lack of cure make this attractive in a high volume setting.

The current work, utilizing fully packaged thermal test vehicles (TTVs), compares TIM1 thermal performance of a PCMA system and organic thermal interface products. The importance of robust PCMA-based processor packaging and the impact on environmental reliability are also presented.

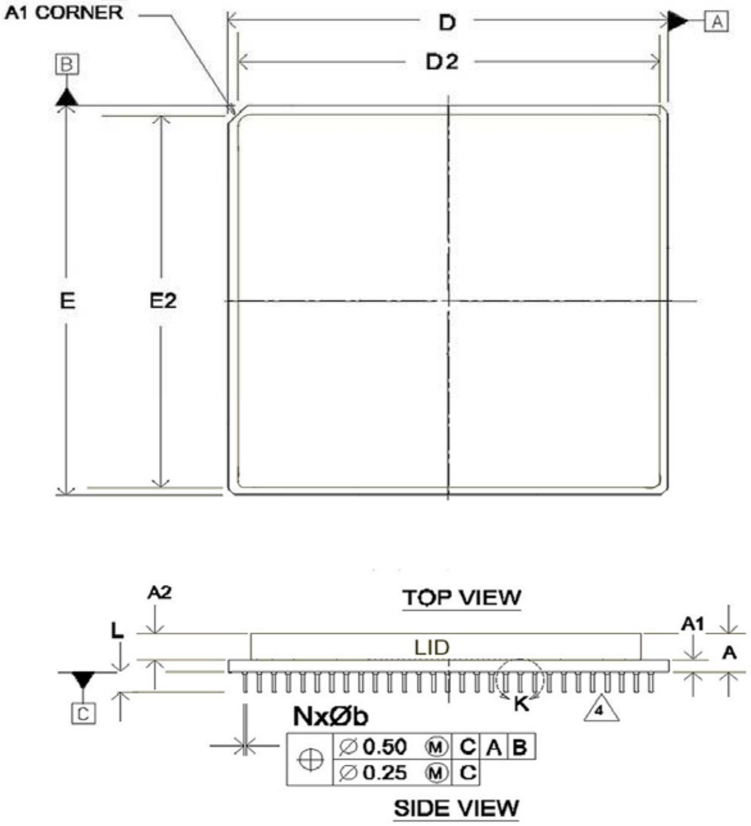
Test Methodology

The TTV (Thermal Test Vehicle) is a non-functional processor package that utilizes multiple heater resistors to simulate the power dissipation of a live processor. Power can be applied to the die to simulate a variety of heat flux dissipation patterns. The TTV's die temperature can be monitored by way of resistive heat sensors. TTVs do a good job of approximating the thermal behavior of the processor; however, there typically are minor differences in power density and power uniformity. These differences can be factored out by the application of TTV-to-CPU correction factors. Our tests utilize an organic FCPGA packaged TTV with a 1.4cm2 die area running at 80 watts. The die was biased for uniform heat flux and die temperature was monitored via the die-center resistive heat sensor.

TTV Examples

Pictured below is an example of a typical TTV along with pictures of a typical AMD organic Opteron processor package. As mentioned earlier, TTVs can be produced to closely simulate processor package geometry. Additionally, minor variations in processor packages can be factored out to expand a particular TTV's application.

Typical TTV Geometry



Typical Organic Opteron FCPGA package

Thermal Interface Materials

Shin-Etsu X23-7783D

X23-7783D thermal interface material is thermal conductive grease that has been successfully used on CPUs, GPUs, PLCs and other temperature sensitive components. Thermal greases offer several advantages including good wetting, ability to conform to the interfaces, possess high bulk thermal conductivity (as compared to other classes of materials) and do not require post dispense processing (e.g. cure).

Chomerics T557

T557 is considered a Polymer-Solder Hybrid (PSH) thermal interface material with two phase change points. To insure optimum performance, the pads were exposed to temperatures above 65ºC during testing for a one time burn-in cycle to achieve lowest thermal impedance by reaching minimum bond-line thickness and maximum surface wet out -per manufacturer's specs. To improve thermal performance of polymer TIMs, polymer matrices such as silicones, phase change resins, etc. are combined with fusible solder fillers to form polymer-solder hybrid (PSH) TIMs. During PSH TIM cure, the solder particles reflow and form networks/columnar structures, thereby providing high thermal conductive pathways through the bulk of the TIM. This in turn enhances the flow of heat between the two interfaces. The contact resistances at the metal-polymer interfaces on the die and the heat sink are also lowered due to fusible solder wetting and adherence to these interfaces.

Indium Solder

An all Indium solder joint is a method utilized to attach a die directly to a lid. This type of interface is superior to Polymer-Solder Hybrids or thermal greases; however, the application of Indium solder material is process intensive requiring gold metallization of the mating surfaces for proper adhesion and a larger bond line thickness will be required to reduce CTE mismatch. Furthermore, the larger bond line thickness increases issues with voiding in the thermal interface.

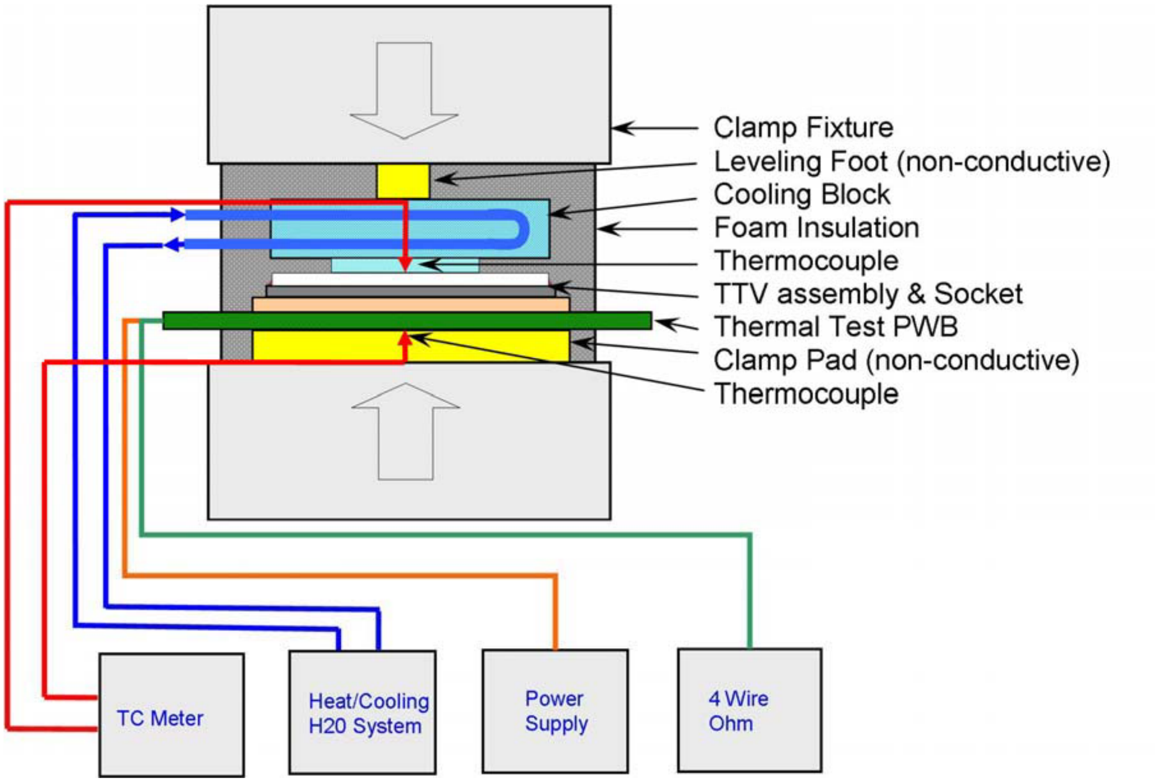
Indigo 1

Indigo1 is a 100% metals TIM with Indium as a primary constituent. It creates a low defect interface between a silicon die and a nickel plated copper IHS. Indigo1 has a melting point between 62 and 65 degrees C, and reflows during the first heat cycle. This reflow forms an interface with both the silicon and nickel, minimizing thermal interface resistance. It is self-adhering, and once applied to the IHS, remains in place until package assembly. Indigo1 is designed to reflow during the heat cycle used to cure the IHS mount adhesive. Indigo also incorporates proprietary mitigants which negate known PCMA failure mechanisms.

Test system overview

The main components of the test system consist of a pneumatic clamp fixture with load cell for adjusting heat sink clamping force and a water block simulating heat sink and maintaining calibration temperature. The water block utilizes alignment pins to insure proper registration of the TTV and thermal test PWB to the rest of the components in the test stack. The TTV die temperature sensor is connected to a 4 wire resistance meter. The TTV die heater modules are connected in parallel and are biased with a load sensing power supply. TTV lid and base temperatures are monitored by thermocouples.

Test system block diagram



Test method

A typical test begins by degreasing the TTV then applying the TIM 1 under test followed by lid attach. The TTV is then inserted into the test fixture and clamp pressure is set to simulate heat sink clamping force under test.

The TTV is then calibrated (usually only once) and is performed with no power to the heating elements. The calibration consists of measuring die sensor resistance (R) with a 4 wire ohm meter at two known temperatures (Typically at room temperature and again at 80C). A water block is utilized to control calibration temp along with two thermocouples to insure a uniform temperature is maintained in the test stack during measurement.

The two measurements give us the sensor calibration slope expressed as (M) ohms/°C, which is linear over the temperature range.

$$M = (R\ (@80°C) - R\ (@20°C)) / (80 - 20)$$

The next phase of the test consists of an un-biased equilibrium measurement of the TTV case temperature T(0) and the die temperature sensor R(0) resistance value.
The TTV die is then biased to the power value under test and the TTV temperature is allowed to equalize for at least 10 minutes.
Then the die resistance RES and package case T(case) temperature are recorded along with power supply voltage (V) and current (I).

From these recorded measurements, junction temperature (Tj) and junction-to-case thermal resistance (Rjc) can be calculated:

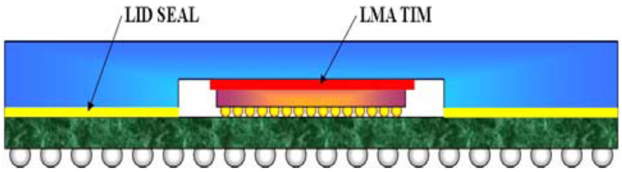
$$Tj = T(0) + \ (RES - R(0)) / m \qquad\qquad Rjc = Tj - T(case) / (V * I)$$

Packaging Considerations

The use of a phase change metal alloy thermal interface system places some specific requirements on the package design. While these requirements are not onerous, they are not typical of commercial microprocessor packages, and must not be ignored.

Environmental Isolation

One packaging requirement is that the PCMA system be somewhat isolated from the environment. This isolation is necessary due to the susceptibility of PCMAs to environmental degradation from corrosion in the presence of both moisture and oxygen. To eliminate this degradation, the system must incorporate some type of moisture barrier to protect the PCMA. This barrier may be an epoxy or silicone adhesive seal around the perimeter of the heat spreader that also holds the spreader to the substrate. A further requirement on this adhesive is that it must allow the heat spreader to align itself to the die when the PCMA is liquefied for the first time. In this way, the package is self aligning for minimum thermal impedance, and the adhesive locks this configuration in by curing after the first PCMA liquefaction.



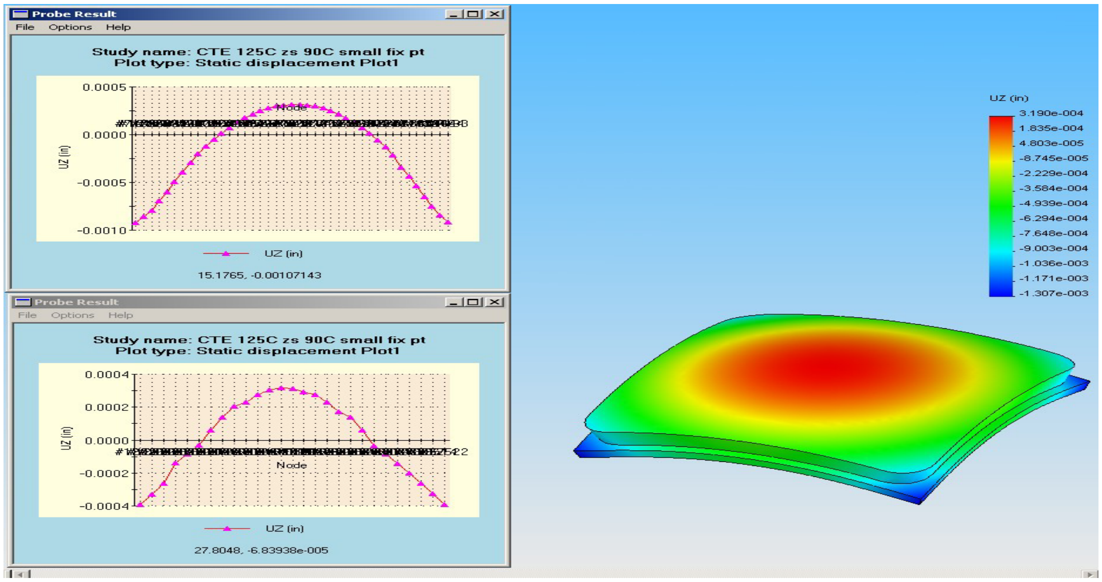
Another packaging requirement unique to PCMA or Low Melt Alloy (LMA) TIMs is the need for package cavity atmosphere control. With non-hermetic or organic sealed packages, some moisture and will leak into the package simply by diffusing through the organic packaging materials. Moisture levels may be maintained at acceptable levels with small amounts of desiccant. These may be deployed as chips, or even included in a particle getter type gel applied to the package cavity interior.
Additionally, certain vapor phase corrosion inhibitors have been demonstrated to be effective at drastically limiting PCMA TIM corrosion. To maximize PCMA TIM lifetime, these materials may also be incorporated in the package cavity as corrosion inhibitor chips or gels.

Vent Defects

When an adhesive is used to mount a cover to a cavity package, expansion of the gas in the cavity may cause venting during adhesive cure. This vent may remain in the adhesive post cure. Various methods may be used to eliminate the vent defect inherent to sealing a cavity package a flowable adhesive. These include leaving a vent in the seal to be filled later with a room temperature cure adhesive, and using a vented cover that is sealed later.

Bondline Thickness (BLT) and "Oil Canning"

Since the BLT attainable with PCMAs is minimal and because of the extreme thermal performance attainable with PCMAs, small changes in package dimensions from Oil Canning or spherical deformation may be significant. The CTE mismatch between the FCPGA and the heat spreader lid may cause the BLT to change slightly as the package temperature is lowered from the adhesive glass transition temperature (Tg). The size of this Oil Canning induced BLT change is dependant upon package variables including component CTEs, adhesive elastic modulus and thickness, and the amplitude of the temperature excursion below the adhesive Tg. This small dimensional instability is not normally significant with low performance TIMs. For FCPGAs, adhesive selection criteria should include Tg, elastic modulus as well as moisture penetration rate.



Study name: CTE 125C zs 90C small fix pt
Plot type: Static displacement Plot1

15.1765, -0.00107143

Study name: CTE 125C zs 90C small fix pt
Plot type: Static displacement Plot1

27.8048, -6.83938e-005

Summary

PCMAs offer high thermal performance due their low bulk and contact impedances; however, because of the enhanced performance of PCMA TIM's, less than optimal packaging design variables are also more likely to produce TIM performance impacts. Considerations normally insignificant to filled greases and epoxies will produce measurable performance impacts on PCMA's. These impacts may be avoided with the incorporation of effective mitigations and with sound package design.